**module dcounter\_3b (clk, set, out);**

**input clk, set;**

**output [2:0] out;**

**reg [2:0] out;**

**always @ (posedge clk)**

**if (~set)**

**out = 3'b111;**

**else**

**out = out - 1;**

**endmodule**

**module test\_dcounter\_3b;**

**reg clk, set;**

**wire [2:0] out;**

**dcounter\_3b dut (clk, set, out);**

**initial begin**

**set = 0;**

**clk = 0;**

**#50**

**set = 1;**

**end**

**always**

**#30 clk = ~clk;**

**endmodule**